Toshiba BiCD Process Integrated Circuit Silicon Monolithic

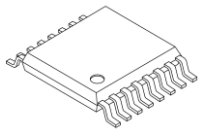
TB67H453FNG/FTG

Single channel H-Bridge driver with integrated current monitoring

1. Description

TB67H453FNG/FTG is a single channel H-Bridge driver with current monitoring function; voltage feedback from ISENSE output pin. Absolute maximum ratings: 50V/3.5A. Capable of controlling 1 brushed DC motor (bidirectional) or 2 brushed DC motors (single direction).

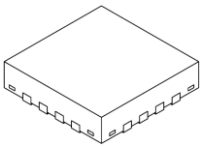
TB67H453FNG



P-HTSSOP16-0505-0.65-002

Weight: 0.06 g (typ.)

TB67H453FTG



P-VQFN16-0303-0.50-001

Weight: 0.02 g (typ.)

2. Features

- Controlling brushed DC motor with integrated H-Bridge.
- Operation voltage range: 4.5 ~ 44 V
- Output current range: 3.5 A(Max)
- Integrated low Rds(on) (H+L=0.6 Ω (typ.))
- Current monitoring function (ISENSE)
- Low power consumption/standby current
- Multiple error detections (Over temperature (TSD), Over current (ISD), Under voltage lockout (UVLO))
- Error detection (TSD/ISD/UVLO) signal output function
- Fully integrated charge pump (external capacitor not required).
- HTSSOP16/VQFN16pin packages with exposed thermal pad.

Note: Please be careful about thermal conditions during use.

Start of commercial production
2024-11

3. Block Diagram

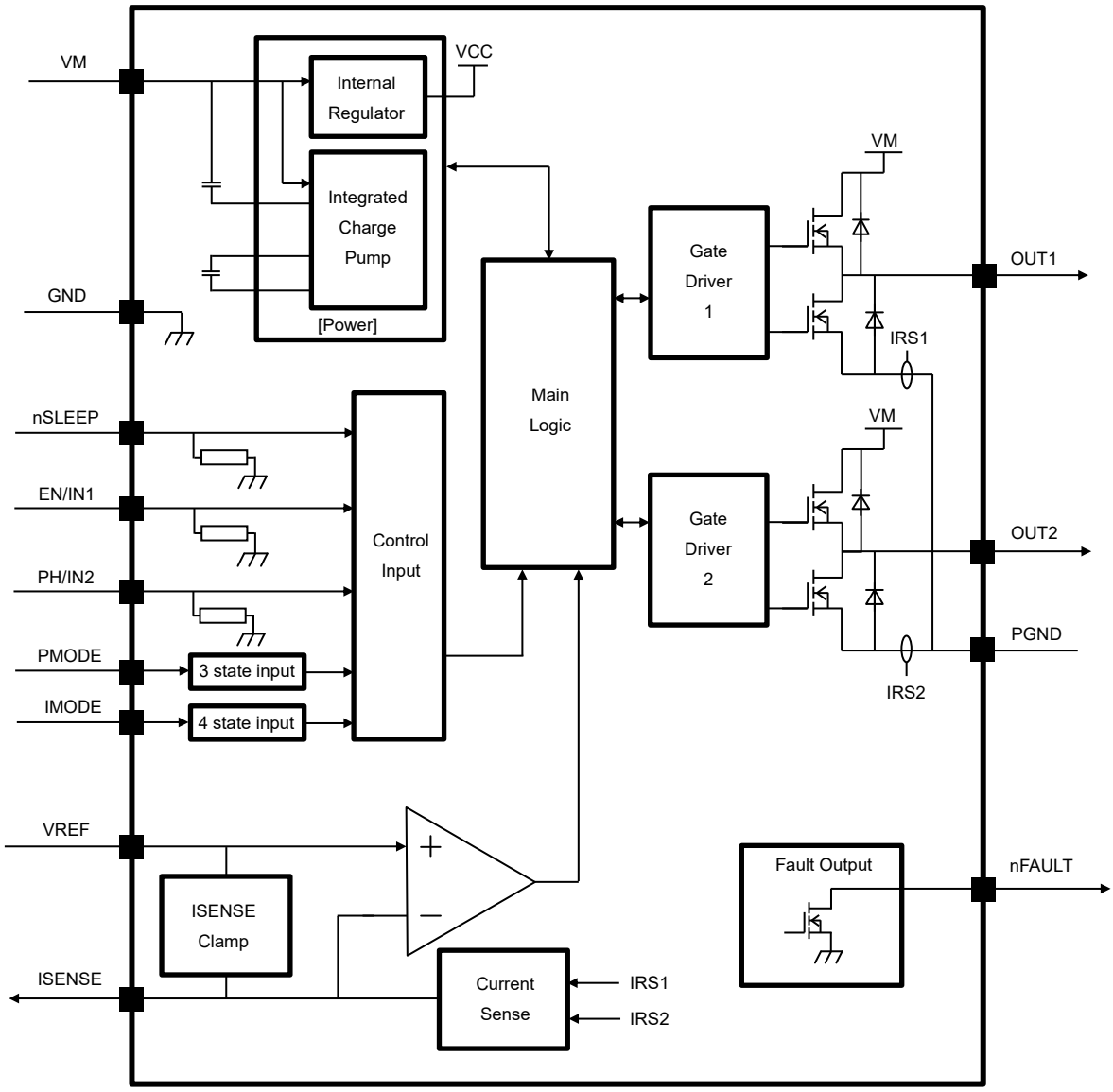


Figure 3.1 Block Diagram

Note: Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purpose.

Note: Extra caution is needed when designing the patterns of the outputs, VM, and GND, PGND to avoid circuit shortage which may cause permanent damage to the device. Also, utmost care should be taken, especially for the pins which run high current (VM, OUT, GND, PGND). If these pins are not wired correctly, not only malfunction may occur, but the device may be destroyed. Logic pins should also be wired correctly otherwise the device may be damaged due to irregular conditions (such as over current); which may lead to damaging or even destroying the device. Take extra caution when designing the patterns and mounting the device.

4. Pin Assignments

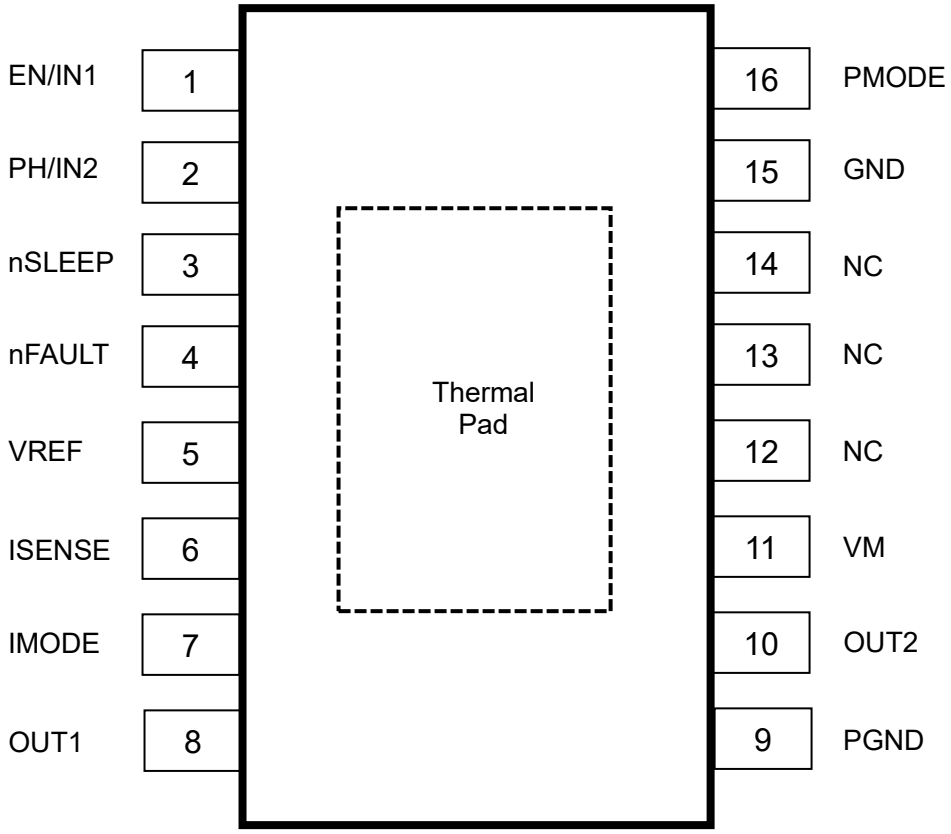


Figure 4.1 TB67S453FNG Pin Assignments

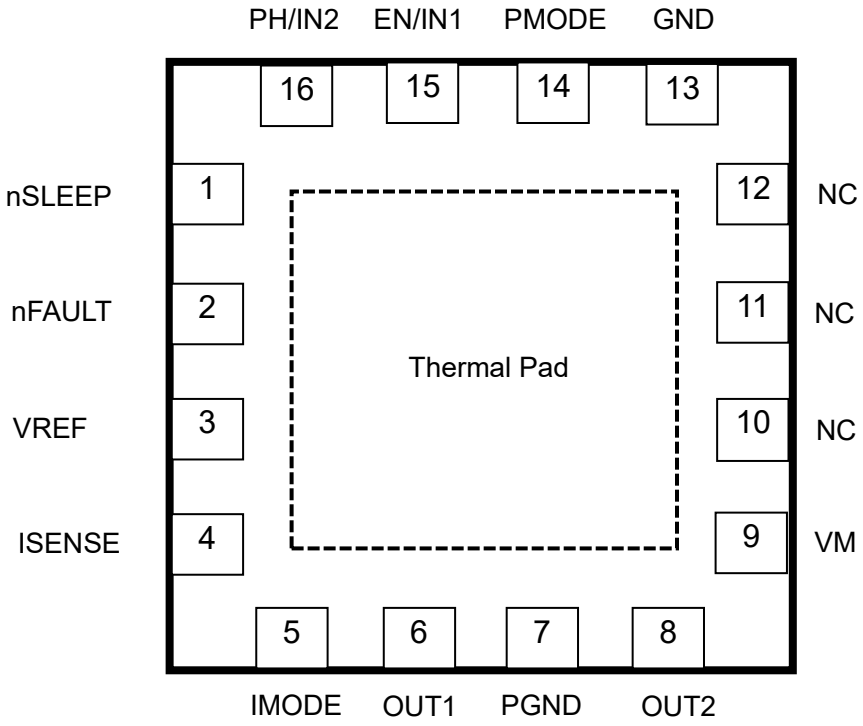


Figure 4.2 TB67H453FTG Pin Assignments

Note: When using the device, always solder the thermal pad to the GND area of the board.

5. Pin Description

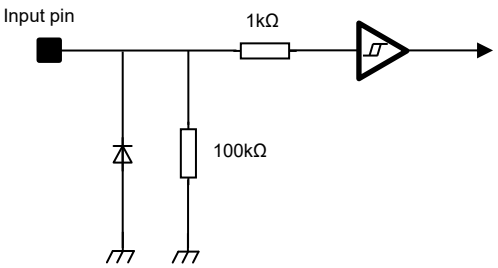
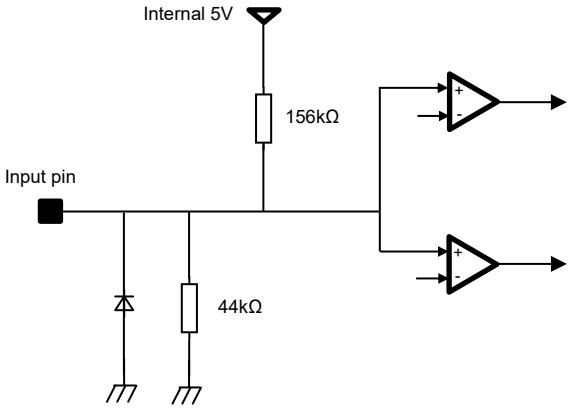
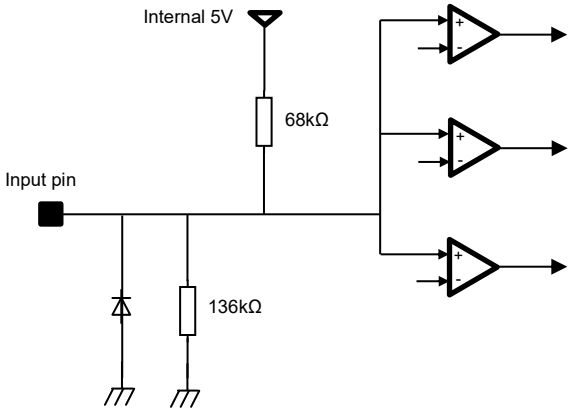
Table 5.1 Pin Description

Pin Name	Package Name		Pin Explanation
	HTSSOP16	VQFN16	
NC	13	11	Non-connection (Use with pin open)
NC	14	12	Non-connection (Use with pin open)
EN/IN1	1	15	H-Bridge control pin (ENABLE/IN1 input)
GND	15	13	GND pin (Connect to board GND area)
IMODE	7	5	Current control mode setting pin
ISENSE	6	4	Current monitoring output pin
nFAULT	4	2	Error detection output pin
nSLEEP	3	1	Sleep (low power consumption mode)/Normal operation setting pin
OUT1	8	6	H-Bridge output pin1
OUT2	10	8	H-Bridge output pin2
PGND	9	7	Power GND pin (Connect to board GND area)
PH/IN2	2	16	H-Bridge control pin (PHASE/IN2 input)
PMODE	16	14	H-Bridge control mode setting pin
NC	12	10	Non-connection (Use with pin open)
VM	11	9	VM power supply pin
VREF	5	3	Output current threshold setting pin
(PAD)	-	-	Thermal pad (Connect to board GND area)

Note: Keep the NC (non-connection) pins open and do not connect any patterns.

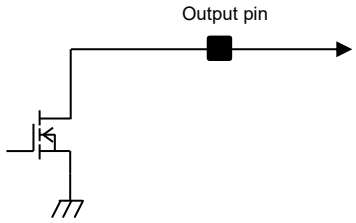
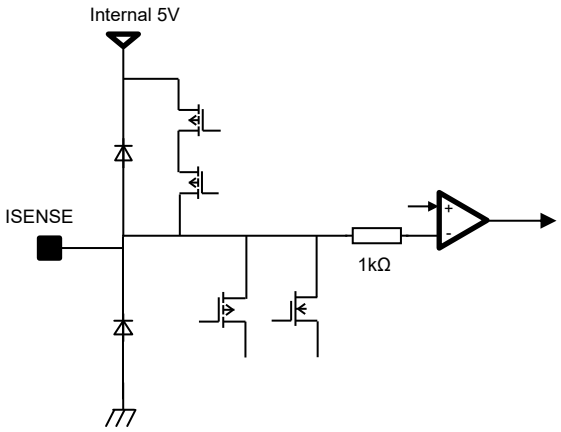
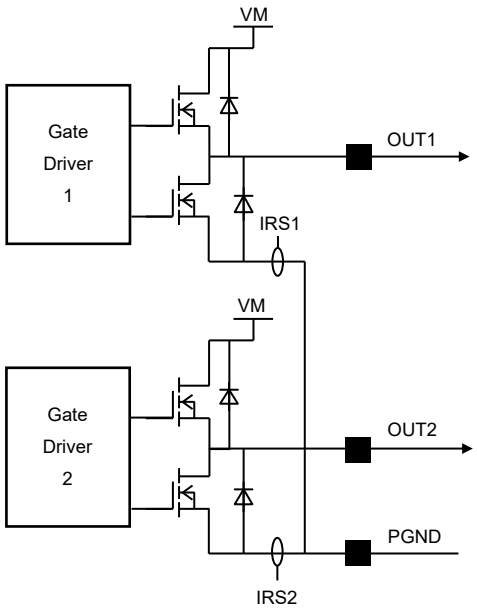
6. Input Output Equivalent Circuit

Table 6.1 Input output equivalent circuit1

Pin Name	Input Output Equivalent Circuit
EN/IN1 PH/IN2 nSLEEP	
PMODE	
IMODE	

Note: The equivalent circuit diagrams may be simplified for explanatory purposes.

Table 6.2 Input output equivalent circuit2

Pin Name	Input Output Equivalent Circuit
nFAULT	
ISENSE	
OUT1 OUT2 PGND	

Note: The equivalent circuit diagrams may be simplified for explanatory purposes.

7. Functional Description

7.1. H-Bridge control mode (PMODE)

TB67H453FNG/FTG controls the H-Bridge with EN/IN1 and PH/IN2 pins. H-Bridge control mode is set by the PMODE pin. The PMODE pin level will be determined when the nSLEEP signal has been applied, and the setting will be locked until the device is set to SLEEP mode. To change the setting of PMODE; set the nSLEEP to Low, and after tSLEEP has surpass, change the PMODE to the new setting. Then, reapply the nSLEEP signal for the device to determine the new setting. PMODE should be set to open when using individual half bridge control mode.

Table 7.1 PMODE setting

PMODE	Function
Low	Phase/Enable control
High	PWM control
Hi-Z (Open)	Individual half bridge control

■Timing chart of PMODE, IMODE settings

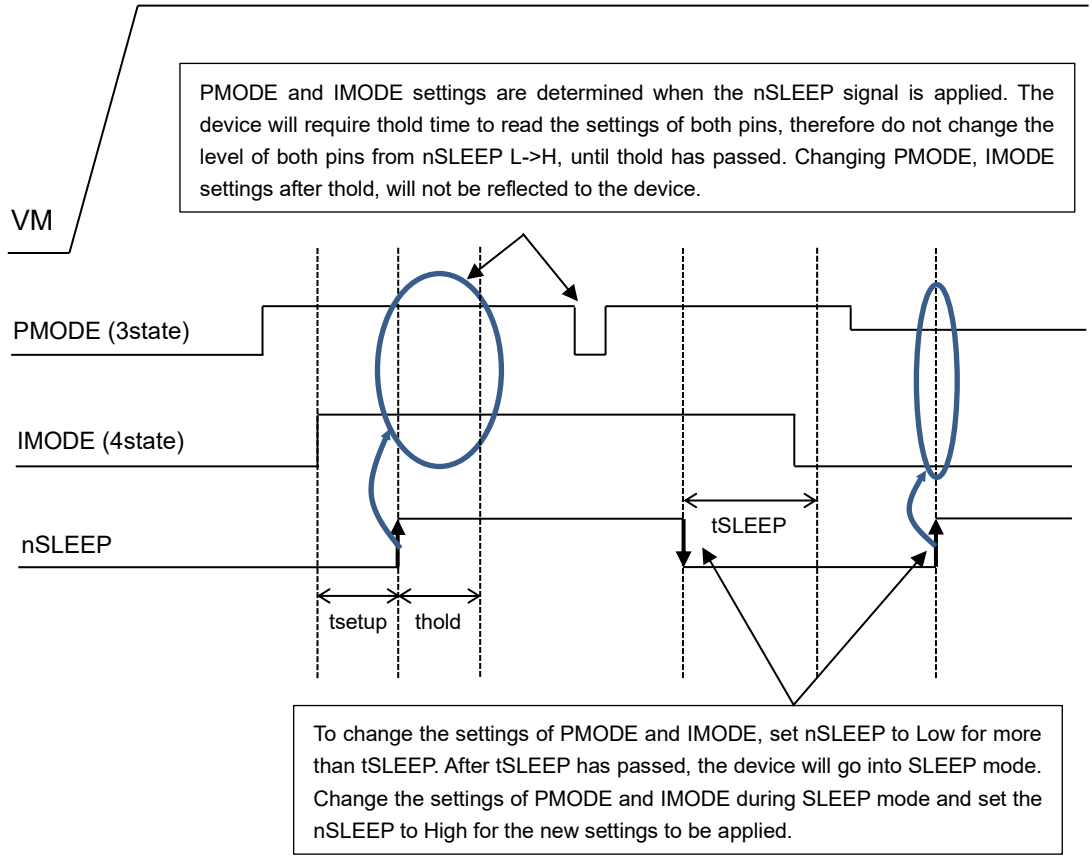


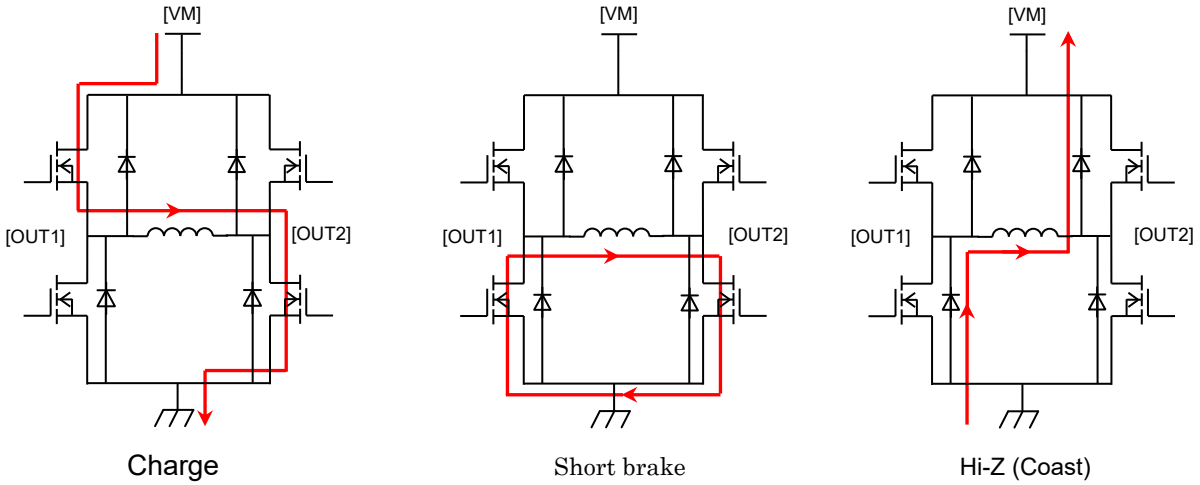
Figure 7.1 PMODE, IMODE settings timing chart

Note: Timing charts may be simplified or omitted for explanatory purposes.

PMODE/IMODE and nSLEEP setup-hold time (reference)
tsetup: 1us(typ.) (designed target value)
thold: 63us(typ.) (designed target value)

7.2. H-Bridge function mode

[Forward] setting



[Reverse] setting

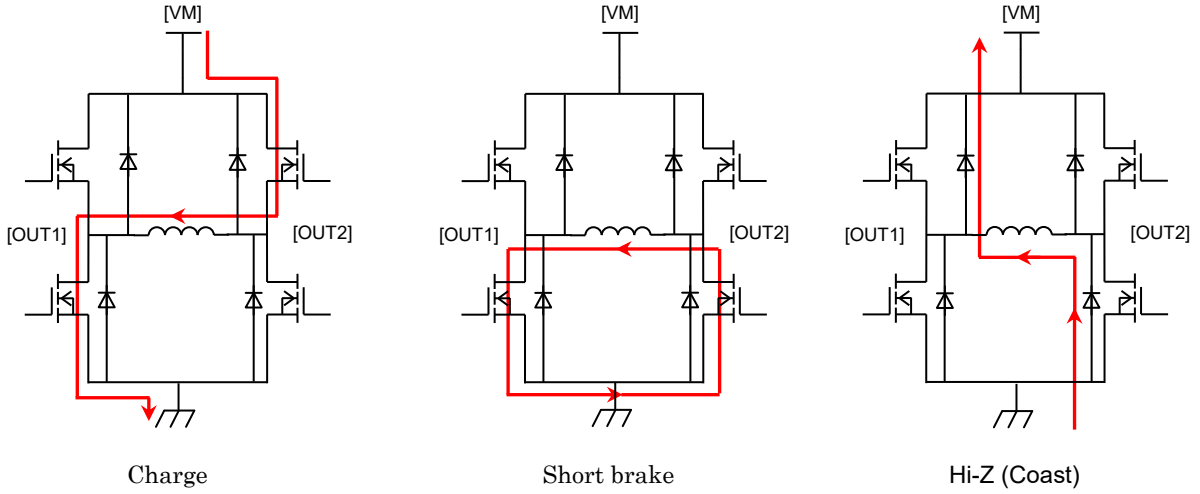


Figure 7.2 H-Bridge function mode

Note: The equivalent circuit diagrams may be simplified for explanatory purposes.

7.2.1. H-Bridge Control (Phase/Enable control mode: PMODE = Low)

The H-Bridge of TB67H453FNG/FTG will be controlled by EN(Enable) and PH(Phase) pin. Pin settings and output functions are as shown below .

Table 7.2.1 Phase/Enable control mode

nSLEEP	EN	PH	OUT1	OUT2	Function
Low	(Don't care)	(Don't care)	Hi-Z	Hi-Z	Sleep mode
High	Low	(Don't care)	Low	Low	Short brake
High	High	Low	Low	High	Reverse (OUT2→OUT1)
High	High	High	High	Low	Forward (OUT1→OUT2)

7.2.2. H-Bridge Control (PWM control mode: PMODE = High)

The H-Bridge of TB67H453FNG/FTG will be controlled by IN1 and IN2 pin. Pin settings and output functions are as shown below .

Table 7.2.2 PWM control mode

nSLEEP	IN1	IN2	OUT1	OUT2	Function
Low	(Don't care)	(Don't care)	Hi-Z	Hi-Z	Sleep mode
High	Low	Low	Hi-Z	Hi-Z	Output off (Coast) mode
High	Low	High	Low	High	Reverse (OUT2→OUT1)
High	High	Low	High	Low	Forward (OUT1→OUT2)
High	High	High	Low	Low	Short brake

7.2.3. H-Bridge Control (Half bridge individual control mode: PMODE = Hi-Z (open))

Each half bridge of TB67H453FNG/FTG will be controlled by INx pin. Pin settings and output functions are as shown below.

Table 7.2.3 Half bridge individual control mode

nSLEEP	INx	OUTx	Function
Low	(Don't care)	Hi-Z	Sleep mode
High	Low	Low	OUTx Low side ON
High	High	High	OUTx High side ON

※x=1 or 2

Current monitoring feature will still be available in Half bridge individual control mode, but since each half bridge is controlled individually, the constant current control will be disabled. Also, when both OUT1 and OUT2 Low side FETs are on, the ISENSE output will show the total current amount.

7.3. Current monitoring function

The ISENSE pin will output a current level proportional to the current flowing to the Low side MOSFETs in the H-Bridge scaled by A(ISENSE). The ISENSE output current can be calculated by the formula below.

ISENSE [μA] = (I(LS1)+I(LS2)) [A] ×A(ISENSE) [μA/A]

The I(LS1) and I(LS2) mentioned in the formula above is only valid when the current is flowing from drain to source in the low side MOSFET. If the current is flowing from source to drain, the value of I(LS1) and/or I(LS2) for that channel is zero. For example, if the H-Bridge is in short brake mode (or slow decay state), the current out of ISENSE is only proportional to the current in one of the low side MOSFETs.

The current is measured by an internal current mirror architecture, which does not require external current sense resistor for the motor output stage. The current mirror architecture allows for the motor current to be sensed in forward, reverse, short brake mode, allowing the continuous current monitoring in a general bidirectional brushed DC motor applications. In coast mode, the current will recirculate and flow from source to drain, which cannot be sensed. However, the current can be monitored by setting to forward, reverse, or short brake mode temporarily and measuring the current before switching back to coast mode again. In Half bridge individual control mode, and both low side MOSFETs have current flowing from drain to source, the ISENSE output will be the sum of the two low side MOSFET currents.

The ISENSE pin should be connected to an external resistor (RISENSE) to GND, in order to generate a proportional voltage (VISENSE) on the ISENSE pin, with the ISENSE analog current output. This allows for the motor current to be measured as the voltage difference across the RISENSE resistor with a standard analog to digital converter (ADC). Also, this device integrates a voltage clamp circuit to limit the VISENSE with respect to the VREF pin voltage, to avoid over voltage occurring to ISENSE pin in case of output over current or unexpected high current events.

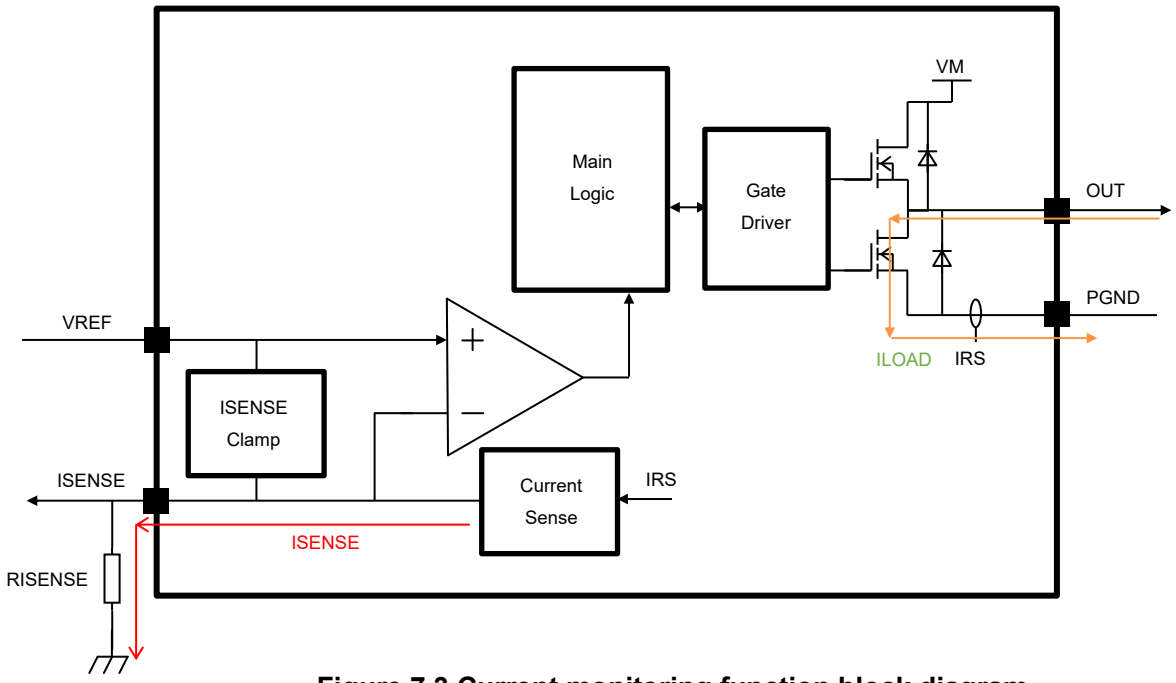


Figure 7.3 Current monitoring function block diagram

Note: The equivalent circuit diagrams may be simplified for explanatory purposes.

7.4. Current control

TB67H453FNG/FTG can select the current control mode by IMODE pin setting. The current control modes are either by constant current PWM mode or fixed off time control. The fixed off time control turns off the output for a certain period of time after the load current reaches the threshold. TB67H453FNG/FTG has an error detection feature where the device monitors any irregular over current; turns off the MOSFETs when detected (ISD). IMODE pin also sets the function of the over current detection (ISD).

The IMODE pin level will be determined when the nSLEEP signal has been applied, and the setting will be locked until the device is set to SLEEP mode. To change the setting of IMODE; set the nSLEEP to Low, and after tSLEEP has surpass, change the IMODE to the new setting. Then, reapply the nSLEEP signal for the device to determine the new setting.

Table 7.4 IMODE setting

IMODE pin setting	Function		nFAULT
	Constant current	Over current	
GND	Fixed off time control	Auto recovery	Over current only
20kΩ pull down	Constant current PWM	Auto recovery	Constant current and over current
62kΩ pull down	Constant current PWM	Latched	Constant current and over current
Hi-Z (open)	Fixed off time control	Latched	Over current only

The constant current threshold (INF) is set by 2 variables; VREF voltage and ISENSE pull down resistor (RISENSE).

INF=VREF/R(ISENSE)×1/A(ISENSE)

For example, to set the constant current threshold to 2.0A (i.e. R(RISENSE)=1.5kΩ 、A(ISENSE)=1000μA/A)

2.0=VREF/1.5kΩ×1/0.001

Therefore, the VREF must be set to 3V.

When the INF threshold is exceeded, the outputs will start the constant current control according to the IMODE setting. Note that the INF comparator has a digital blanking time (Dtblk) and an analog blanking time (Atblk) to avoid being affected by inrush current and/or external noise.

7.5. Digital blanking time(Dtblk) and analog blanking time(Atblk)

(Example) Constant current setting: Fixed off time control

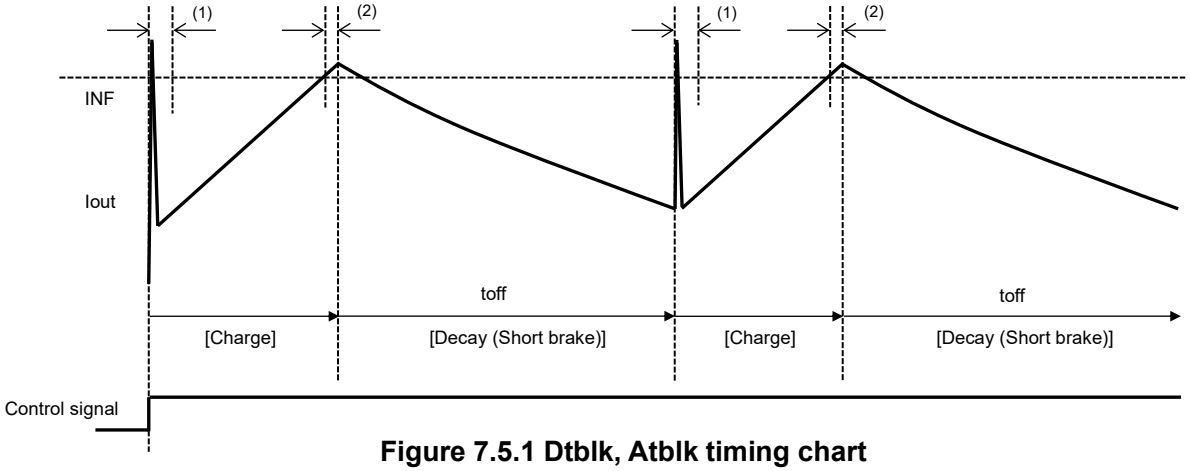


Figure 7.5.1 Dtblk, Atblk timing chart

Note: Timing charts may be simplified or omitted for explanatory purposes.

TB67H453FNG/FTG has a fixed value filtering time to reject incoming noise or spike current caused by the motor operation. Dtblk will start from the beginning of each cycle, and Atblk will start after the current reaches the constant current threshold.

(1) Digital tblank (Dtblk): To avoid detecting spike currents when H-Bridge switches from Decay to Charge.
(2) Analog tblank (Atblk): To avoid detecting incoming noise when the load current is close to the constant current threshold (INF)
(Please refer to the electric specification for detailed values of each blanking time.)

(Example) Constant current control : Constant current PWM control(IN signal controlled)

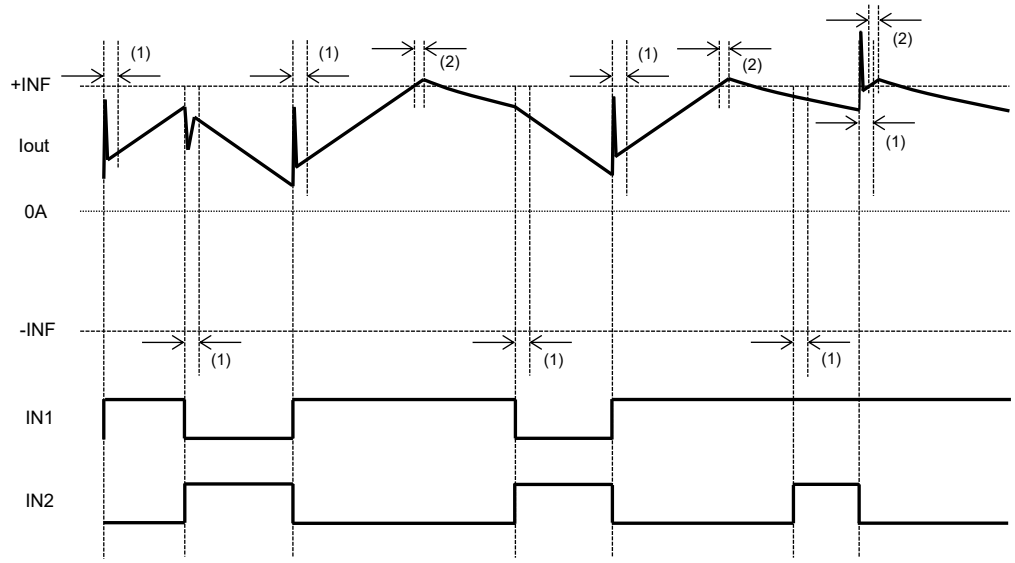


Figure 7.5.2 Blanking time example

(The above timing charts shows current as (+) when the current flows from OUT1 to OUT2 in Charge state.)
Note: Timing charts may be simplified or omitted for explanatory purposes.
Dtblk will occur at the beginning of each cycle. For example, in Constant current PWM mode which requires logic input signal for current control; the Dtblk will occur at starting from every signal polarity change (Low⇔ High) of the control signals. Dtblk will filter the INF detection for charge (plus) current. Dtblk and Atblk are individual blanking time.

7.6. Constant current function: Fixed off time control

When controlled in Fixed off time; the H-bridge will switch to short brake (both low side MOSFETs ON) for a fixed off time (toff), when the motor current (Iout) exceeds the current threshold (INF). After toff, the outputs are re-enabled according to the control signal inputs unless Iout is still above INF level. If Iout is still above INF after toff, the H-bridge will enter another period of short brake (both low side MOSFETs ON) for toff.

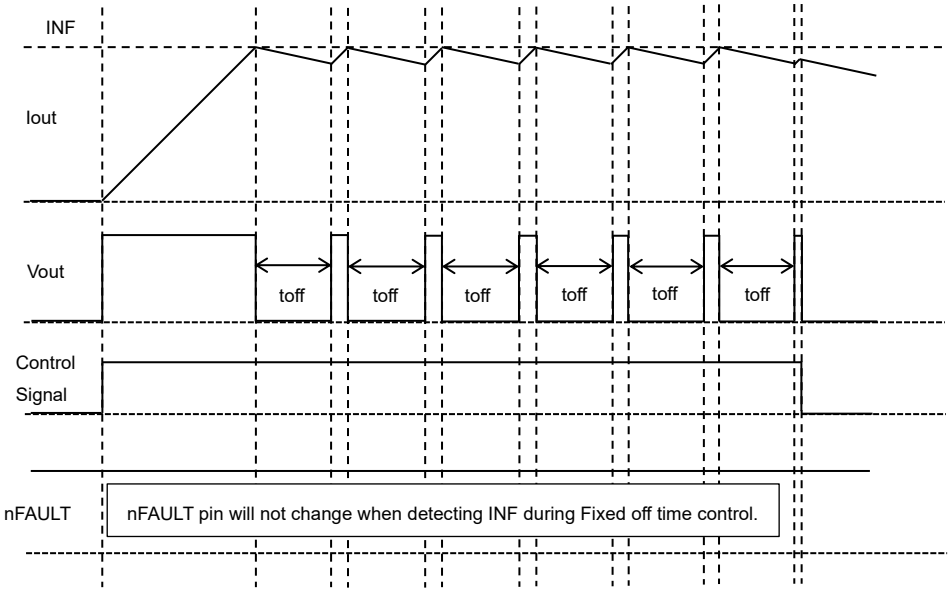
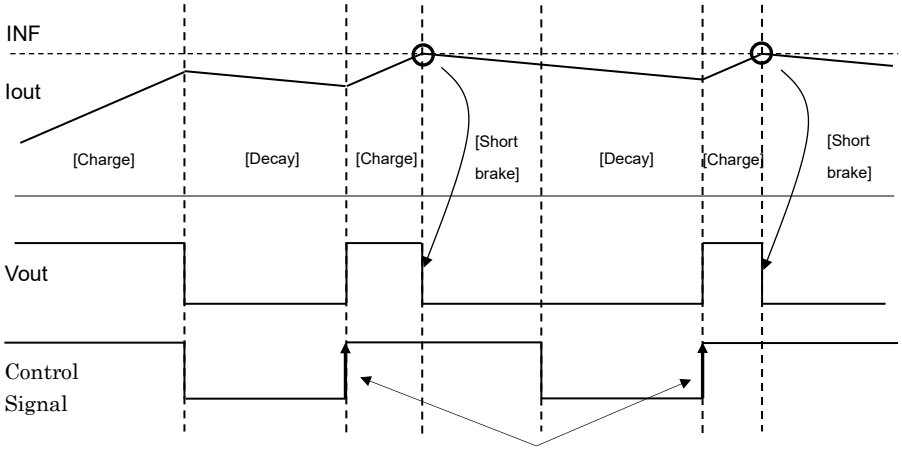


Figure 7.6 Fixed off time control timing chart example

Note: Timing charts may be simplified or omitted for explanatory purposes.

7.7. Constant current function: Constant current PWM control

When controlled in Constant current PWM; the H-bridge will switch to short brake (both low side MOSFETs ON) until the next control signal input edge of EN/IN1 or PH/IN2 is asserted, after the motor current (Iout) exceeds the current threshold (INF).



The H-bridge will switch to short brake after the motor current exceeds the current threshold; until the next control signal input edge of EN/IN1 or PH/IN2 is asserted. To reset the outputs after short brake, the next control signal input edge is required.

Figure 7.7.1 Constant current PWM control timing chart example 1

Note: Timing charts may be simplified or omitted for explanatory purposes.

In Constant current PWM control, the device will also indicate whenever the motor current (Iout) exceeds the current threshold (INF) by pulling the nFAULT pin to Low. This can be used to determine when the device outputs will differ from the input control signals. nFAULT will be released when the next control input signal edge is asserted, and the outputs are reset.

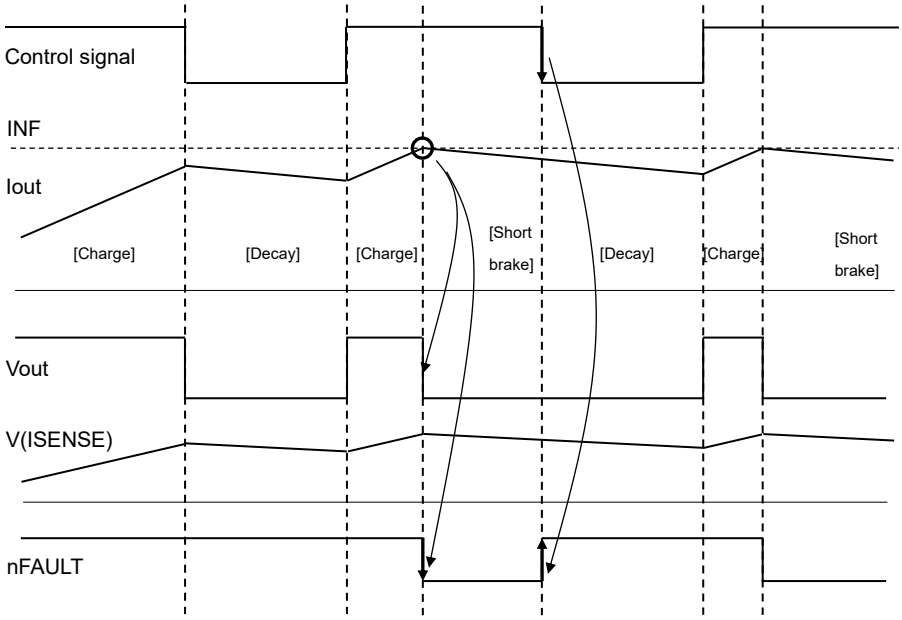


Figure 7.7.2 Constant current PWM control timing chart example 2

Note: Timing charts may be simplified or omitted for explanatory purposes.

No device functionality will be affected when the nFAULT pin outputs Low during constant current PWM control. The nFAULT pin is only used as an output signal pin to indicate that the motor current (Iout) exceeded the current threshold (INF), and the device will continue normal operation.

When the device is set to constant current PWM control via IMODE pin setting, the nFAULT pin will show Low for both Iout>INF, and when detecting an over current (ISD). The nFAULT pin can be compared with the control input signals to tell two detections apart.

The Iout>INF status can only be achieved when the control signals are set for either forward or reverse state, described in the H-bridge control table (7.2. H-Bridge function mode). If the nFAULT pin shows Low and the control signal inputs are set to either Hi-Z or short brake, then the device has detected an over current (ISD).

The current control can be disabled by connecting ISENSE pin directly to GND, and setting the VREF pin voltage higher than GND (if current monitoring is not required). If the current monitoring is required, set the VREF voltage and RISENSE so that the VISENSE never reaches the current threshold set by VREF. In Half bridge individual control mode (PMODE=Hi-Z), the internal current control is automatically disabled, since the outputs are operating individually.

8. Error detection features

TB67H453FNG/FTG has an over current detection, over temperature detection, and under voltage lockout detection for error detection features.

8.1. Over current detection (ISD)

When a current flows through the integrated MOSFETs and exceeds the over current detection threshold (ISDth), the device detects an over current state and turns off the H-Bridge. Latch or auto recovery function after detecting the over current can be set via the IMODE pin. The nFAULT pin will show Low when over current is detected.

8.1.1. When PMODE pin is set to Low or High:

When the function of the ISD is set to auto recovery; the H-Bridge will turn off after detecting the over current, and will stay turned off for a period of time (tRETRY). During this period, the nFAULT will show Low. After tRETRY period has passed, the H-Bridge will be turned on depending on the EN/IN1, PH/IN2 pin settings. If the over current state has not been resolved after the tRETRY period has passed, the device will detect the over current again and turns off the H-Bridge. (If so, the nFAULT will show Low again.) If the over current state has been resolved during tRETRY period, the device will restart the normal operation.

When the function of the ISD is set to latch; the H-Bridge will turn off after detecting the over current, and will stay turned off until the VM power is turned off and reasserted, or the nSLEEP signal is applied to reset the error detection state. The nFAULT pin will show Low until the device is reset.

When the H bridge control is set to half bridge individual control mode (PMODE=Hi-Z), the over current (ISD) behavior will be different. If an over current is detected, the corresponding half bridge will be disabled and the nFAULT pin will show Low. The other half bridge will continue the normal operation. If an over current is detected in both half bridges, both half bridges will be disabled and the nFAULT pin will show Low.

When PMODE=Hi-Z and IMODE=GND or 20kΩ pulldown: Both half bridges share the same over current retry (tRETRY) timer. If an over current event occurs first in one half bridge, and then later in the other half bridge, but before tRETRY has expired, the retry timer for the first half bridge will be reset to tRETRY and both half bridges will enable again after the retry timer expires.

Example: [PMODE = Low or High], IMODE(ISD)=Auto recovery

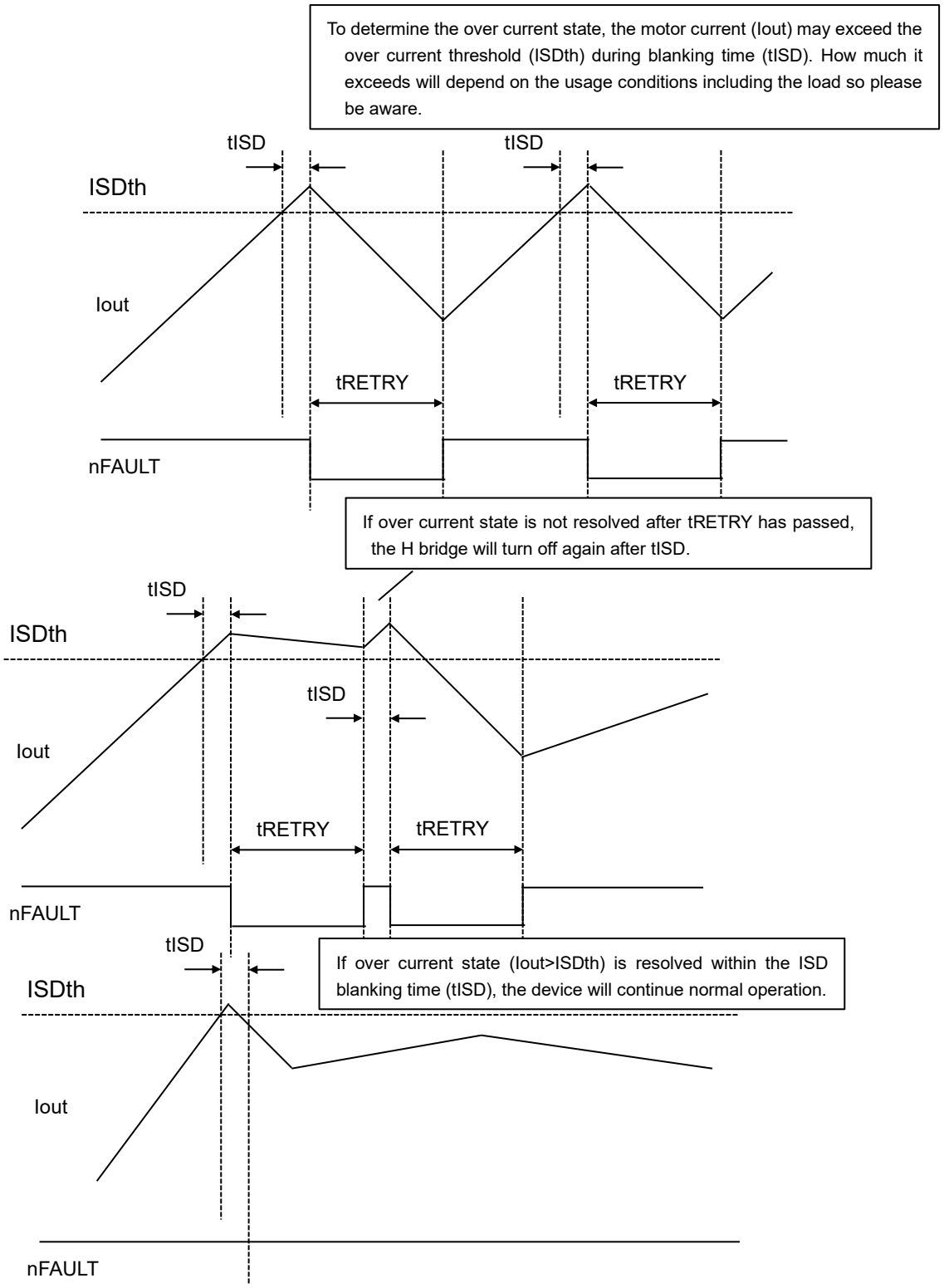


Figure 8.1.1 Over current detection function timing chart example [PMODE = Low or High]

Note: Timing charts may be simplified or omitted for explanatory purposes.

8.1.2. When PMODE pin is set to Hi-Z(open):

When the device is set to half bridge individual control mode, and the ISD is set to auto recovery; both half bridges share the same over current retry timer tRETRY. For example, if one of the half bridge detects an over current state and turns off, and the other half bridge also detects an over current state before tRETRY passes, then the internal tRETRY timer will be reset and both half bridge will be turned off until the tRETRY passes from the secondary half bridge ISD detection.

Example: [PMODE = Hi-Z (open)], IMODE(ISD)=Auto Recovery

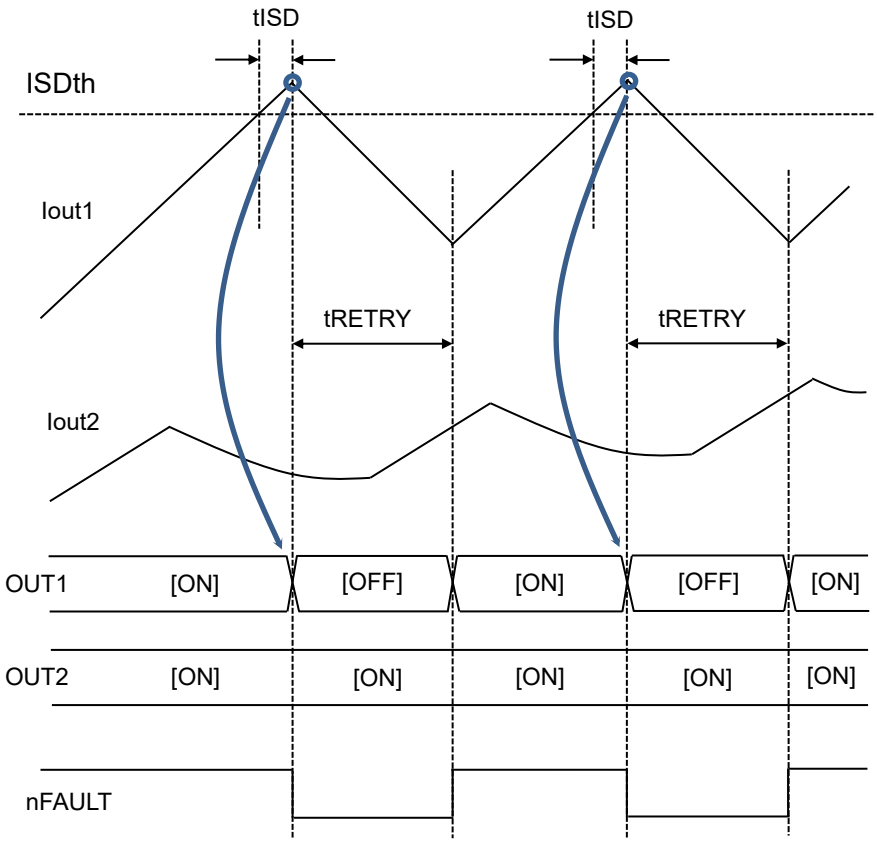


Figure 8.1.2 Over current detection timing chart example 1 [PMODE = Hi-Z]

Note: Timing charts may be simplified or omitted for explanatory purposes.

When the H-bridge setting is set to half bridge individual control mode; if an over current is detected, the corresponding half bridge will be disabled.
For example, when the OUT1 half bridge detects an over current, the OUT1 output will turn off while the OUT2 output will continue normal operation as shown in the timing chart example above.

Note that the nFAULT pin shares the same internal timer, therefore if either of the half bridge detects an over current, the pin will show Low level.

Example: [PMODE = Hi-Z], IMODE(ISD)=Auto Recovery

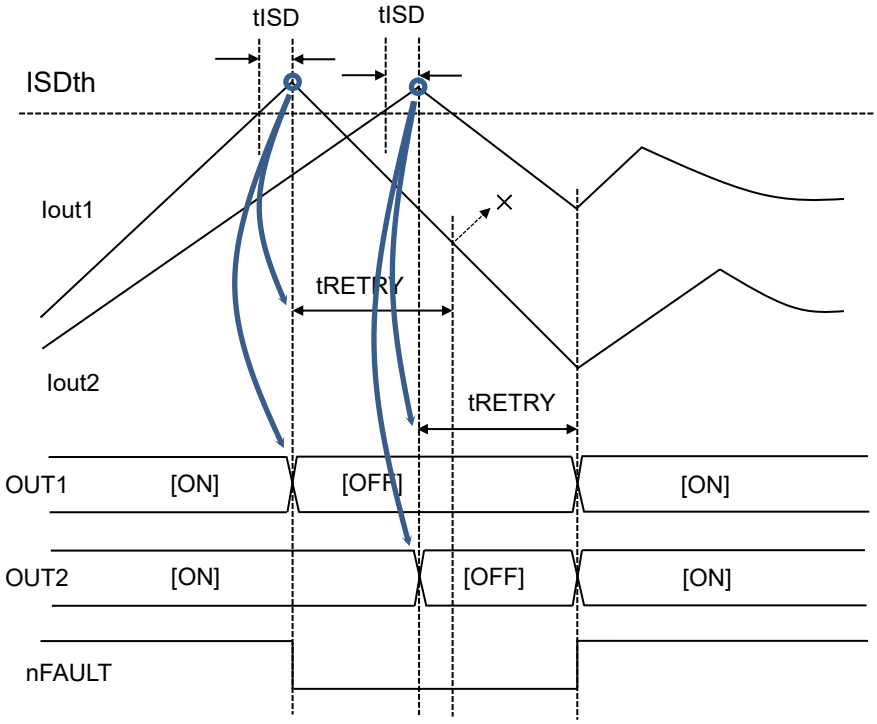


Figure 8.1.3 Over current detection timing chart example 2 [PMODE = Hi-Z]

Note: Timing charts may be simplified or omitted for explanatory purposes.

For example (as shown above), first the OUT1 half bridge detects an over current and turns off the output. Since the ISD function is set to auto recovery, the internal tRETRY timer starts to count up. The OUT2 half bridge will keep operating, but it also detects an over current before the tRETRY time passes.

Both OUT1 and OUT2 half bridges share the same over current retry (tRETRY) timer. If an over current event occurs first in one half bridge, and then later in the other half bridge, but before tRETRY has expired, the retry timer for the first half bridge will be reset to tRETRY and both half bridges will enable again after the retry timer expires.

The nFAULT will show Low level once the OUT1 half bridge detects an over current, but will continue showing Low level if the OUT2 also detects an over current before the retry timer expires.

8.2. Thermal shutdown / Over temperature detection (TSD)

When the die temperature exceeds the internal over temperature threshold (TSDth), the H-bridge output will be disabled, and the nFAULT pin will show Low level. Normal operation will resume once the over temperature situation is resolved, and the die temperature drops to the recovery threshold (TSD(rec)).

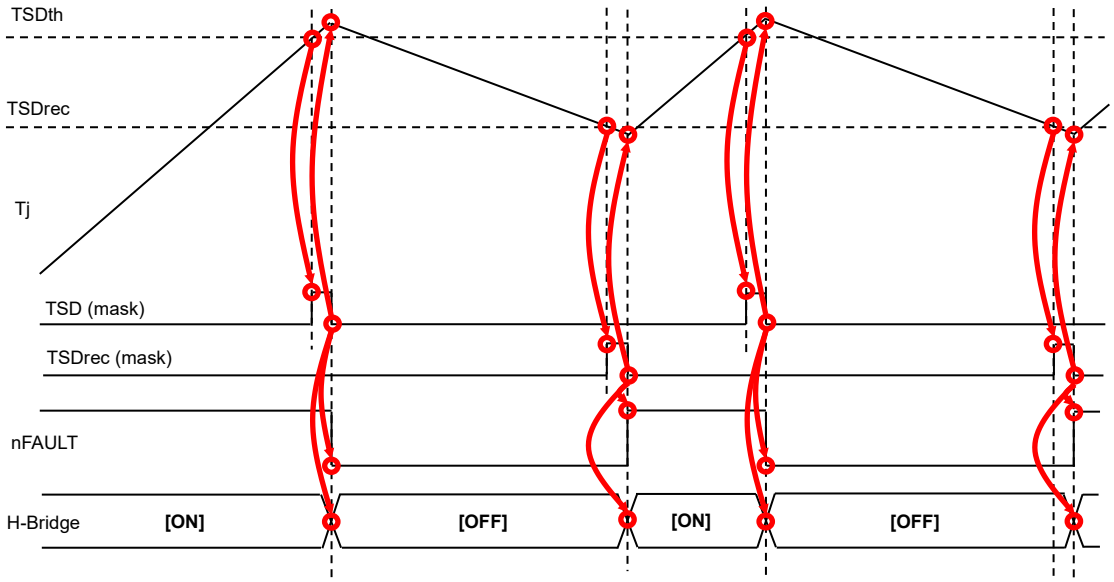


Figure 8.2 Over temperature detection timing chart

Note: Timing charts may be simplified or omitted for explanatory purposes.

Noise filtering time for TSD detection and TSD recovery:

The TSD circuit has two filtering time to avoid false detection which may be caused by external noise or internal circuit switching.
・TSD(mask): Filtering time to avoid false detection mainly caused by external noise, TSD(mask) =5μs(typ.)(design target). When the die temperature exceeds the TSD threshold for more than TSD(mask) period, the device will detect TSD.
・TSDrec(mask) Filtering time to avoid false detection mainly caused by internal circuit switching, TSDrec(mask)=5μs(typ.)(design target). When the die temperature drops below the TSD recovery threshold for more than TSDrec(mask) period, the device will resume to normal operation.
Note: Design target values are for reference, and is not guaranteed.

Initial temperature monitoring:

The initial temperature monitoring circuit will determine if the die temperature is safe to operate, once the VM power is applied. If the die temperature is higher then the TSD recovery threshold TSD(rec), the device will not start the power up sequence and stays until the die temperature drops below the TSD(rec). Note that the initial temperature monitoring has a variation in performance therefore the startup sequence will start when junction temperature is below 120℃.

Cautions on Overcurrent Shutdown (ISD) and Thermal Shutdown (TSD)

The ISD and TSD circuits are only intended to provide temporary protection against irregular conditions such as an output short-circuit; they do not necessarily guarantee the complete IC safety.
If the device is used beyond the specified operating ranges, these circuits may not operate properly: then the device may be damaged due to an output short-circuit.
The ISD circuit is only intended to provide a temporary protection against an output short-circuit. If such a condition persists for a long time, the device may be damaged due to overstress. Overcurrent conditions must be removed immediately by external hardware.

8.3. Undervoltage Lockout (UVLO)

To avoid malfunction in low voltage condition, the H-bridge is turned off when the VM voltage is lower than the UVLO threshold (VUVLO). The nFAULT pin will show Low level during UVLO condition. The internal charge pump will not operate when the UVLO is detected. Normal operation will resume when the VM voltage exceeds the UVLO threshold.

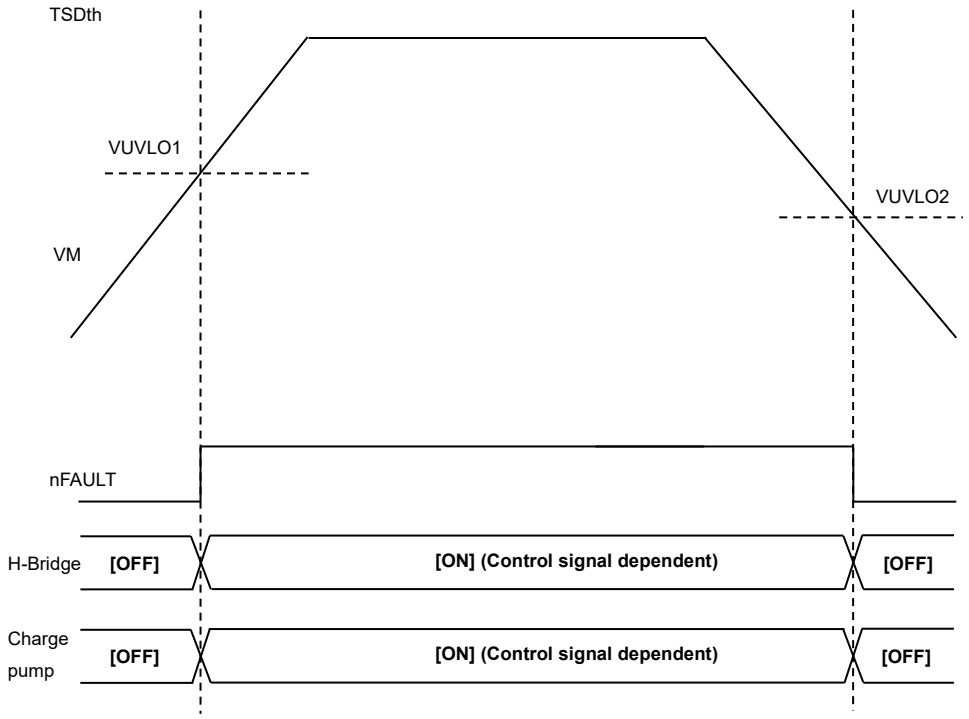


Figure 8.3 Under voltage lockout timing chart example

Note: Timing charts may be simplified or omitted for explanatory purposes.

8.4. Error detection output (nFAULT)

When TB67H453FNG/FTG detects an error condition, the device will signal out via the nFAULT pin.

Table 8.4.1 nFAULT function

nFAULT	Function
Low	Error detection
Hi-Z	Normal operation

The nFAULT behavior is shown below.

Table 8.4.2 nFAULT / Error detection function

Characteristics	Detect condition	Pin output	H-Bridge status	Recovery condition
Constant current detection (INF)	IMODE=20kΩpulldown, or 62kΩpulldown, and Iout>INF	nFAULT=Low	Active (Short brake mode)	Control input signal edge
VM Undervoltage lockout (UVLO)	VM<VUVLO	nFAULT=Low	Output off (Disabled)	VM>VUVLO
Over current detection (ISD)	Iout>ISDth	nFAULT=Low	Output off (Disabled)	tRETRY (Auto recovery setting) or reset (Latch setting); Set by IMODE
Over temperature detection (TSD)	Tj>TSDth	nFAULT=Low	Output off (Disabled)	Tj < TSDrec

9. SLEEP (Low power consumption) mode: nSLEEP

TB67H453FNG/FTG can be set to sleep (low power consumption) mode using the nSLEEP pin.

Table 9 nSLEEP function

nSLEEP	Function
Low	Sleep (Low power consumption) mode
High	Normal operation mode

Sleep mode is entered by setting the nSLEEP to Low and waiting for tSLEEP to elapse. If the nSLEEP is set to High before tSLEEP passes, the device will keep operating in normal operation mode. In sleep mode, the H-bridge, internal charge pump, internal VCC regulator, and other circuits will be disabled to lower the power consumption. The device will not respond to any inputs besides the nSLEEP pin while in low power consumption sleep mode.

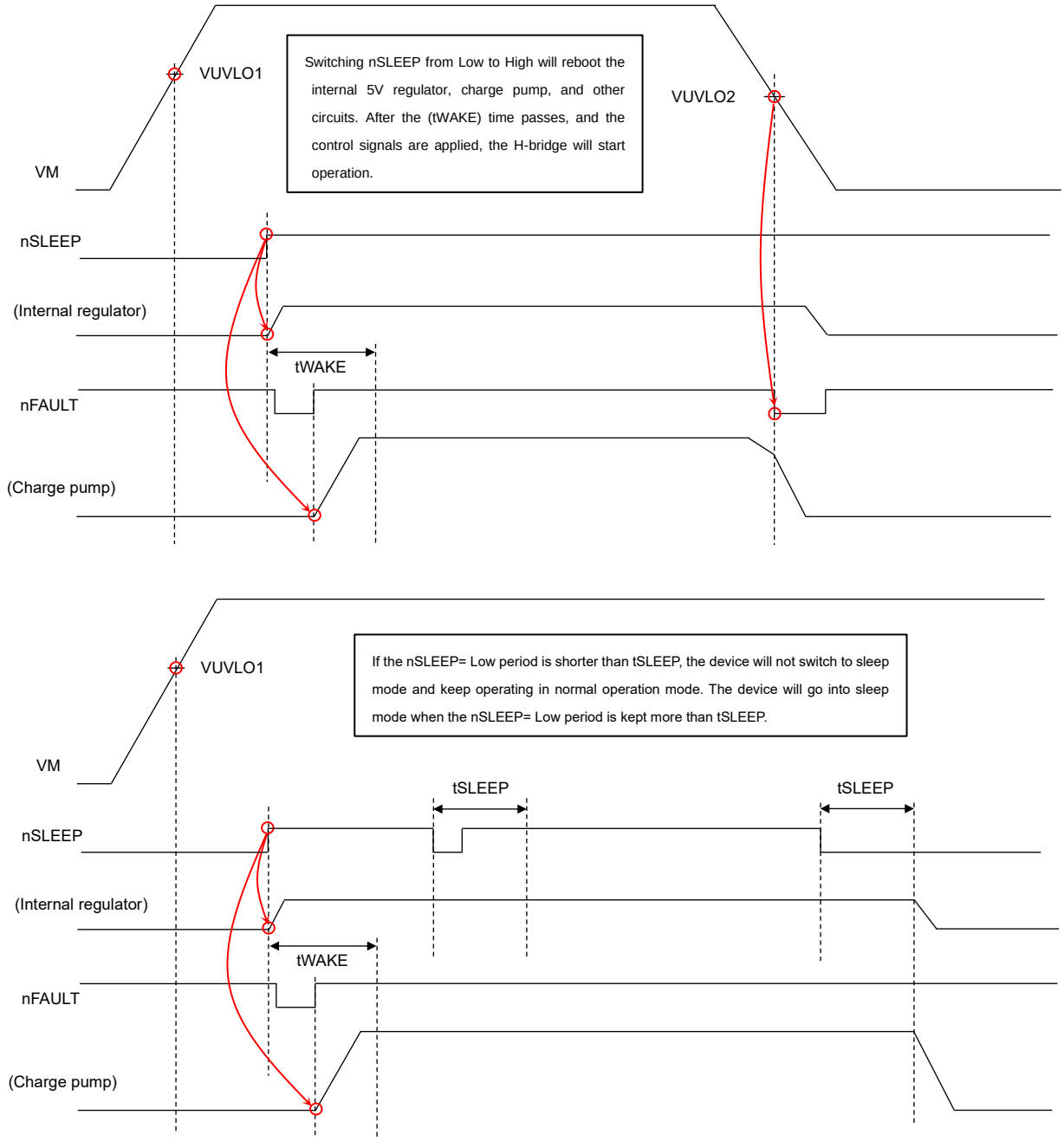


Figure 9 SLEEP function timing chart example

Note: Timing charts may be simplified or omitted for explanatory purposes.

10. Absolute Maximum Ratings(Ta=25℃)

Table 10 Absolute Maximum Ratings

Characteristics	Symbol	Rating	Unit	Remarks
Motor power supply	VM	50	V	-
Motor output voltage	Vout	50	V	OUT1, OUT2
Motor output current	Iout	3.5	A	OUT1, OUT2 (Note1)
Logic input voltage	VIN	6.0	V	EN/IN1, PH/IN2, IMODE, PMODE, nSLEEP
Logic output volage	VLO	6.0	V	nFAULT
Logic output pin inflow current	ILO	6	mA	nFAULT
Logic output pin inflow current (pulse)	ILO (pulse)	15	mA	nFAULT
ISENSE pin voltage	VISENSE	6.0	V	-
VREF pin voltage	VREF	6.0	V	-
Power dissipation	PD	2.5	W	HTSSOP16 (Note2)
		2.5	W	VQFN16 (Note3)
Storage temperature	Tstg	-55 ~ 150	°C	-
Junction temperature	Tj(max)	150	°C	-

Note1: Usually, the maximum current value at the time should use 70% or less of the absolute maximum ratings for a standard on thermal rating. The maximum output current may be further limited in view of thermal considerations, depending on ambient temperature and board conditions.

Note2, Note3: When mounted to a PCB (JEDEC 4layer) (Ta = 25°C)
When Ta exceeds 25°C, it is necessary to do the de-rating with 20mW/°C.
Ta: Ambient temperature
Tj: Junction temperature while the IC is active. The maximum junction temperature is limited by the thermal shutdown (TSD) circuitry. It is advisable to keep the maximum current below a certain level so that the maximum junction temperature, Tj (MAX), will not exceed 125°C.

Caution) Absolute maximum ratings

The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings. Exceeding the rating (s) may cause device breakdown, damage or deterioration, and may result in injury by explosion or combustion. The value of even one parameter of the absolute maximum ratings should not be exceeded under any circumstances. This device does not have overvoltage detection circuit. Therefore, the device is damaged if a voltage exceeding its rated maximum is applied. All voltage ratings, including supply voltages, must always be followed. The other notes and considerations described later should also be referred to.

IC Mounting

Do not insert devices incorrectly or in the wrong orientation. Otherwise, it may cause breakdown, damage and/or deterioration of the device.

11. Operating Ranges(Ta=-40 to 125°C)

Table 11 Operating Ranges

Characteristics	Symbol	Min	Typ.	Max	Unit	Remarks
Motor power supply	VM	4.5	-	44	V	-
Motor output current	Iout	-	-	3.5	A	(Note1)
Logic input pin voltage	VIN	-	-	5.5	V	EN/IN1, PH/IN2, IMODE, PMODE, nSLEEP
PWM frequency	fPWM	-	-	100	kHz	EN/IN1, PH/IN2 (Note2)
Logic output pin voltage	VLO	-	-	5.5	V	nFAULT
Logic output pin inflow current	ILO	-	-	5	mA	nFAULT
ISENSE pin current	ISENSE	-	-	3	mA	-
VREF pin voltage	VREF	0	-	3.6	V	-

Note1: Maximum current for actual usage may be limited by the operating circumstances such as operating conditions (operation voltage, load, ambient temperature, board design, etc.).

Note2: Maximum PWM frequency for actual usage may be limited by the operating circumstances such as operating conditions (operation voltage, load, ambient temperature, board design, etc.).

12. Electrical Characteristics1 (-40≤Tj≤150℃, 4.5V≤VM≤44V, unless otherwise specified)

Table 122 Electrical Characteristics1

Characteristics		Symbol	Test condition	Min	Typ.	Max	Unit
Logic input pin voltage	High	VIN(H)	EN/IN1, PH/IN2, nSLEEP	1.5	-	5.5	V
	Low	VIN(L)	EN/IN1, PH/IN2, nSLEEP, VM<5V	0	-	0.7	V
			EN/IN1, PH/IN2, nSLEEP, VM≥5V	0	-	0.8	V
Logic input pin hysteresis voltage		VIN(HYS)	EN/IN1, PH/IN2	-	200	-	mV
			nSLEEP	-	50	-	
Logic input pin current	HIGH	IIN(H)	VIN(H) = 5.0 V	-	50	75	μA
	LOW	IIN(L)	VIN(L) = 0 V	-5	-	5	μA
Logic input pin pulldown resistor		RPD	EN/IN1, PH/IN2, nSLEEP, to GND	-	100	-	kΩ
PMODE input voltage	High	VPMD(H)	PMODE	1.5	-	5.5	V
	Hi-Z	VPMD(M)1	PMODE (Externally applied)	1.0	1.05	1.1	V
		VPMD(M)2	PMODE (Internally generated)	0.95	1.1	1.2	
	Low	VPMD(L)	PMODE	0	-	0.65	V
PMODE input current	High	IPMD(H)	PMODE=5.0V	-	113	150	μA
	Hi-Z	IPMD(M)	PMODE=1.1V	-5	-	5	μA
	Low	IPMD(L)	PMODE=0V	-50	-32	-	μA
PMODE pin pullup resistor		RPMD(PU)	to internal 5V	-	156	-	kΩ
PMODE pin pulldown resistor		RPMD(PD)	to GND	-	44	-	kΩ

Note: When the logic signal is applied to the device while the VM power supply is not asserted; the device is designed not to function. But for safe usage please apply the logic signal after the VM power supply is asserted and the VM voltage reaches the proper operating range.

Note: VIN(H) is defined as the VIN voltage that causes the outputs (OUT pins) to change when a pin under test is gradually raised from 0 V.VIN(L) is defined as the VIN voltage that causes the outputs (OUT1 pin, OUT2 pin to change when the pin is then gradually lowered. The difference between VIN(H) and VIN(L) is defined as the VIN(HYS).

13. Electrical Characteristics2 (-40≤Tj≤150℃, 4.5V≤VM≤44V, unless otherwise specified)

Table 133 Electrical Characteristics2

Characteristics		Symbol	Test condition	Min	Typ.	Max	Unit
IMODE setting range	Setting 4	VIMD(4)	IMODE pin, voltage regulation	2.5	-	5.5	V
	Setting 3	VIMD(3)	IMODE pin, resistor regulation	57.6	62	66.4	kΩ
	Setting 2	VIMD(2)	IMODE pin, resistor regulation	18.6	20	21.4	kΩ
	Setting 1	VIMD(1)	IMODE pin, voltage regulation	0	-	0.45	V
IMODE pin pullup resistor		RIMD(PU)	to internal 5V	-	68	-	kΩ
IMODE pin pulldown resistor		RIMD(PD)	to GND	-	136	-	kΩ
Logic output pin voltage		VLO	nFAULT pin, ILO=5.0mA	-	-	0.3	V
Logic output pin inflow current		ILO	nFAULT pin, VLO=5.0V	-2	-	2	μA
Motor output pin High side MOSFET on resistance		Ron(H)	OUT1, OUT2 pin, Iout=1A、Tj=25℃	-	0.3	0.375	Ω
Motor output pin Low side MOSFET on resistance		Ron(L)	OUT1, OUT2 pin, Iout=-1A、Tj=25℃	-	0.3	0.375	Ω
Motor output pin High side MOSFET leak current		ILEAK(H)	VM=44V, OUT1, OUT2=0V	-1	-	1	μA
Motor output pin Low side MOSFET leak current		ILEAK(L)	VM=44V, OUT1, OUT2=44V	-1	-	1	μA
Current mirror scaling factor		AISENSE	Iout＝1.0A	-	1000	-	μA/A
Current mirror scaling error		AERR1	Iout<0.15A, 5.5V≤VM≤44V -40℃≤Tj<125℃	-7.5	-	7.5	mA
		AERR2	Iout<0.15A, 5.5V≤VM≤44V 125℃≤Tj<150℃	-10	-	10	mA
		AERR3	0.15A≤Iout<0.5A, 5.5V≤VM≤44V -40℃≤Tj<125℃	-5	-	5	%
		AERR4	0.15A≤Iout<0.5A, 5.5V≤VM≤44V 125℃≤Tj<150℃	-6.5	-	6.5	%
		AERR5	0.5A≤Iout≤2.0A, 5.5V≤VM≤44V, -40℃≤Tj<125℃	-4	-	4	%
		AERR6	0.5A≤Iout≤2.0A, 5.5V≤VM≤44V, 125℃≤Tj<150℃	-5	-	5	%
Output current setting error		Iout(det)1	Iout<0.5A, RISENSE=1kΩ, 5.5V≤VM≤44V	-25	-	25	mA
		Iout(det)2	0.5A≤Iout≤2.0A, RISENSE=1kΩ, 5.5V≤VM≤44V, -40℃≤Tj<125℃	-5	-	5	%
		Iout(det)3	0.5A≤Iout≤2.0A, RISENSE=1kΩ, 5.5V≤VM≤44V, 125℃≤Tj<150℃	-6	-	6	%

14. Electrical Characteristics3 (-40≤Tj≤150℃, 4.5V≤VM≤44V, unless otherwise specified)

Table 144 Electrical Characteristics3

Characteristics		Symbol	Test condition	Min	Typ.	Max	Unit
Body diode forward voltage		VSD	Source-drain current=1A	-	0.9	-	V
Power dissipation	SLEEP	IM1	VM=24V, nSLEEP=0V Tj=25℃	-	0.75	1	μA
		IM2	nSLEEP=0V	-	-	5	μA
	ACTIVE	IM3	VM=24V, nSLEEP=5.0V, EN/IN1=PH/IN2=0V	-	3	7	mA
VREF input current		IREF	VREF=3.6V	-	-	1	μA
UVLO threshold voltage		VUVLO1	VM power on	3.8	4.0	4.2	V
		VUVLO2	VM power off	3.6	3.8	4.0	V
UVLO hysteresis voltage		VUVLOhys	-	-	0.2	-	V
Over current shutdown threshold		ISDth	-	3.5	5.5	-	A
Over temperature shutdown threshold		TSDth	-	150	165	180	℃
Over temperature shutdown recovery threshold		TSD(rec)	-	125	-	150	℃

Back-EMF

While a motor is rotating, there is a timing at which power is fed back to the power supply. At that timing, the motor current recirculates back to the power supply due to the effect of the motor back-EMF.
If the power supply does not have enough sink capability, the power supply and output pins of the device might rise above the rated voltages. The magnitude of the motor back-EMF varies with usage conditions and motor characteristics. It must be fully verified that there is no risk that this device or other components will be damaged or fail due to the motor back-EMF.

15. AC Electrical Characteristics3 (-40≤Tj≤150℃, 4.5V≤VM≤44V, unless otherwise specified)

Table 155 AC Electrical Characteristics

Characteristics	Symbol	Test condition	Min	Typ.	Max	Unit
Wakeup time	tWAKE	VM>VUVLO, nSLEEP=5V	-	-	1.5	ms
Sleep mode setting time	tSLEEP	VM>VUVLO, nSLEEP=0V	-	0.025	1.0	ms
Output rise time	tr	VM=24V, OUTx rising 10% to 90%	145	180	255	ns
Output fall time	tf	VM=24V, OUTx falling 90% to 10%	75	105	145	ns
Input to output propagation delay	tPD	EN/IN1, PH/IN2 to OUTx	380	550	720	ns
Minimum logic input pulse width	tLOG(min)	EN/IN1, PH/IN2	500	-	-	ns
Output dead time	tDEAD	Body diode conducting	-	300	-	ns
Fixed Off-time period	tOFF	-	-	25	-	μs
Current monitoring delay time	tDELAY	-	-	1.6	-	μs
Analog blanking time	At(BLK)	-	-	0.6	-	μs
Digital blanking time	Dt(BLK)	-	-	0.938	-	μs
UVLO deglitch time	tUVLO	-	-	10	-	μs
Over current deglitch time	tISD	-	-	3	-	μs
Over current retry time	tRETRY	-	-	2	-	ms

Note: x=1 or 2

AC Electrical Specifications timing chart

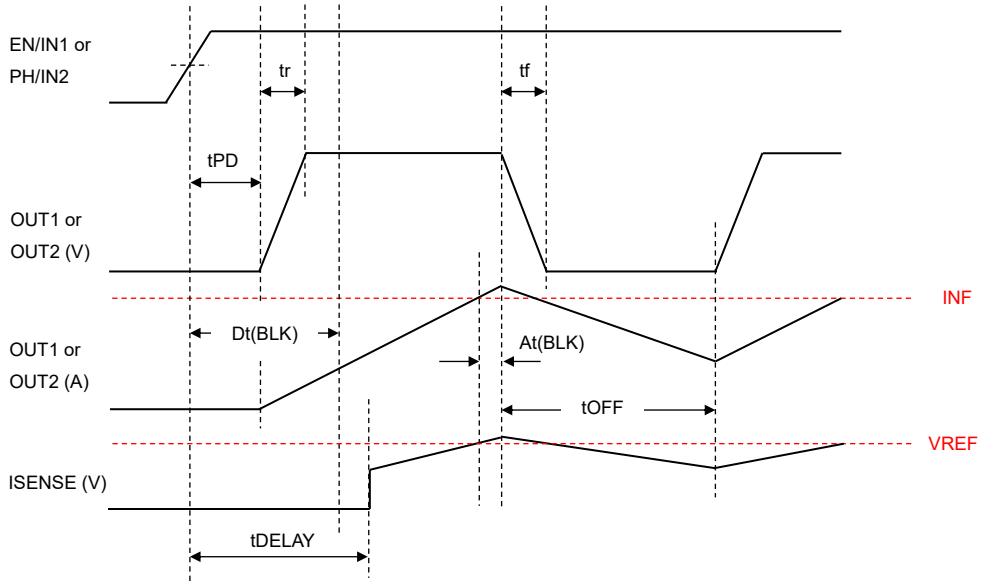


Figure 15 AC electrical specification timing chart

Note: Timing charts may be simplified or omitted for explanatory purposes.

16. PD–Ta graph (For reference)

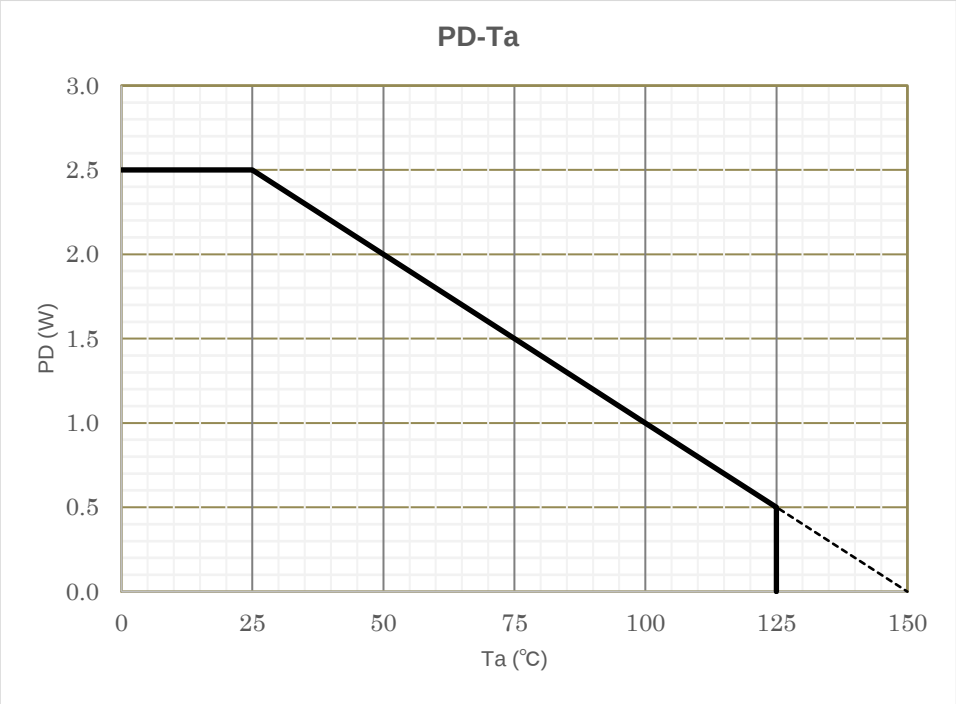


Figure16 When mounted to a JEDEC 4 layered PCB

Note: The graph shown above is for reference and is not guaranteed.

17. Application circuit example

17.1. 1-brushed DC motor connection example

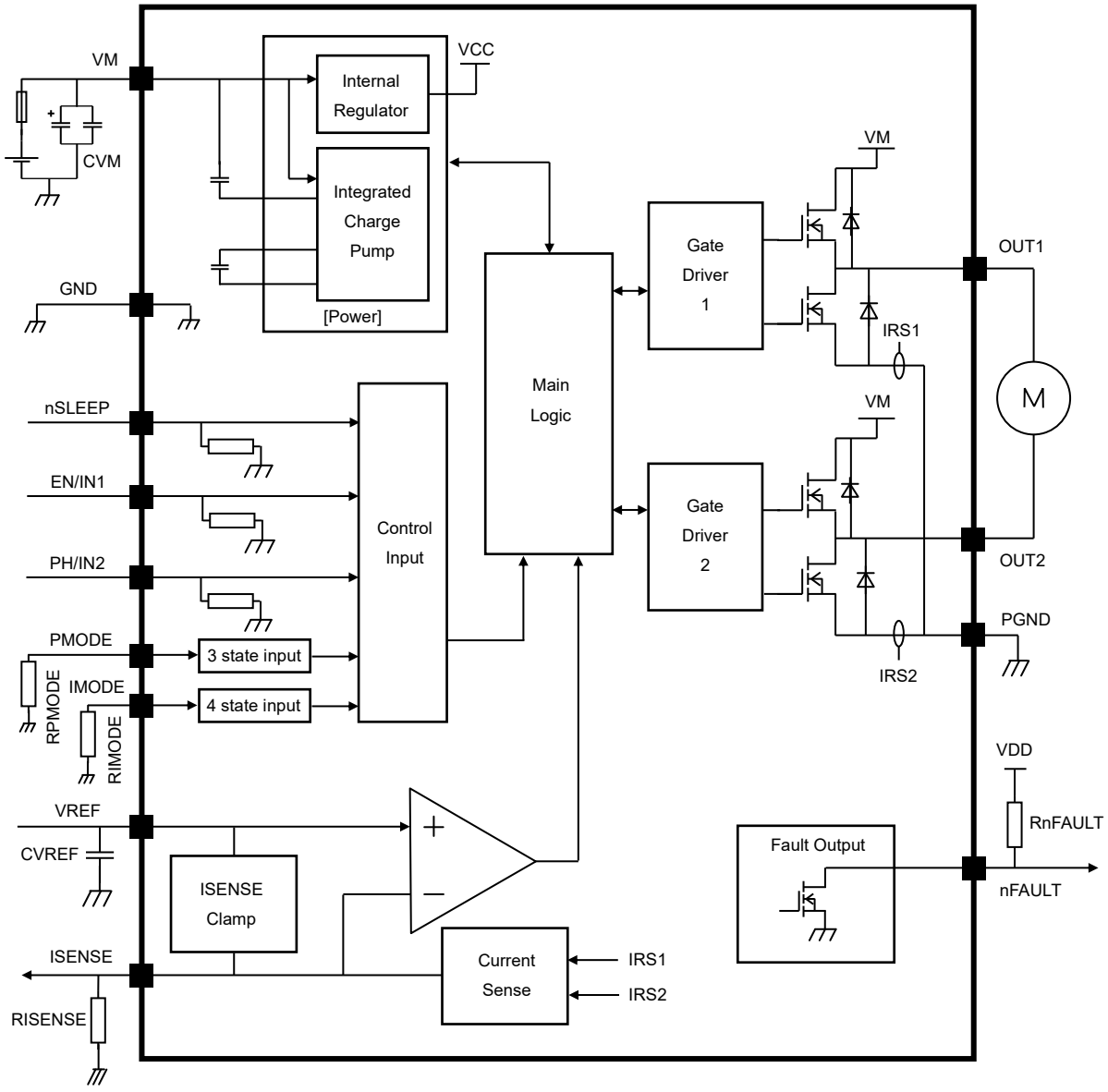


Figure 17.1 Single brushed DC motor connection example

The application circuit example is for refence and is not guranteed.

Table 17.1 External component value example

Symbol	Component	Value
CVM	Electrolytic capacitor + ceramic capacitor (in parallel)	47 µF+0.1µF
CVREF	Ceramic capacitor	0.1 µF
RIMODE	Resistor	Detailed information in “Current control” / IMODE setting
RPMODE	Resistor	Detailed information in “H-bridge mode” / PMODE setting
RnFAULT	Resistor	Pullup resistor, ILO≤5mA
RISENSE	Resistor	Detailed information in “Current monitoring” / “Current control”

Note: Values described in the table is for reference and should be optimized for each usage conditions.

17.2. Half bridge individual control mode (2-brushed DC motor connection example)

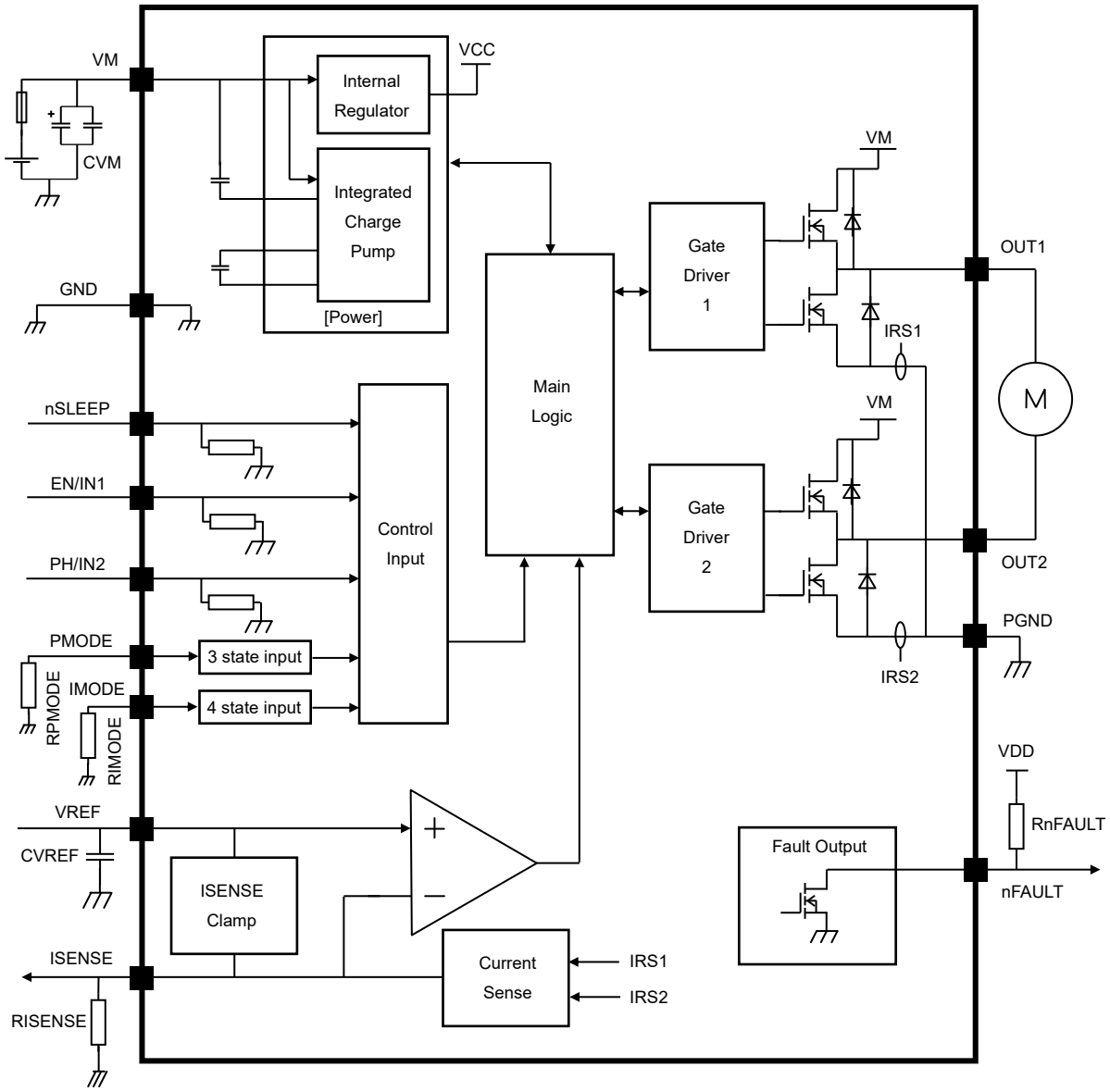


Figure 17.2 2-brushed DC motor connection example

The application circuit example is for refence and is not guranteed.

Table 17.2 External component value example

Symbol	Component	Value
CVM	Electrolytic capacitor + ceramic capacitor (in parallel)	47 µF+0.1µF
CVREF	Ceramic capacitor	0.1 µF
RIMODE	Resistor	Detailed information in “Current control” / IMODE setting
RPMODE	Resistor	Detailed information in “H-bridge mode” / PMODE setting
RnFAULT	Resistor	Pullup resistor, ILO≤5mA
RISENSE	Resistor	Detailed information in “Current monitoring” / “Current control”

Note: Values described in the table is for reference and should be optimised for each usage conditions.

18. Package Information

18.1. Package Dimensions (P-VQFN16-0303-0.50-001)

Unit: mm

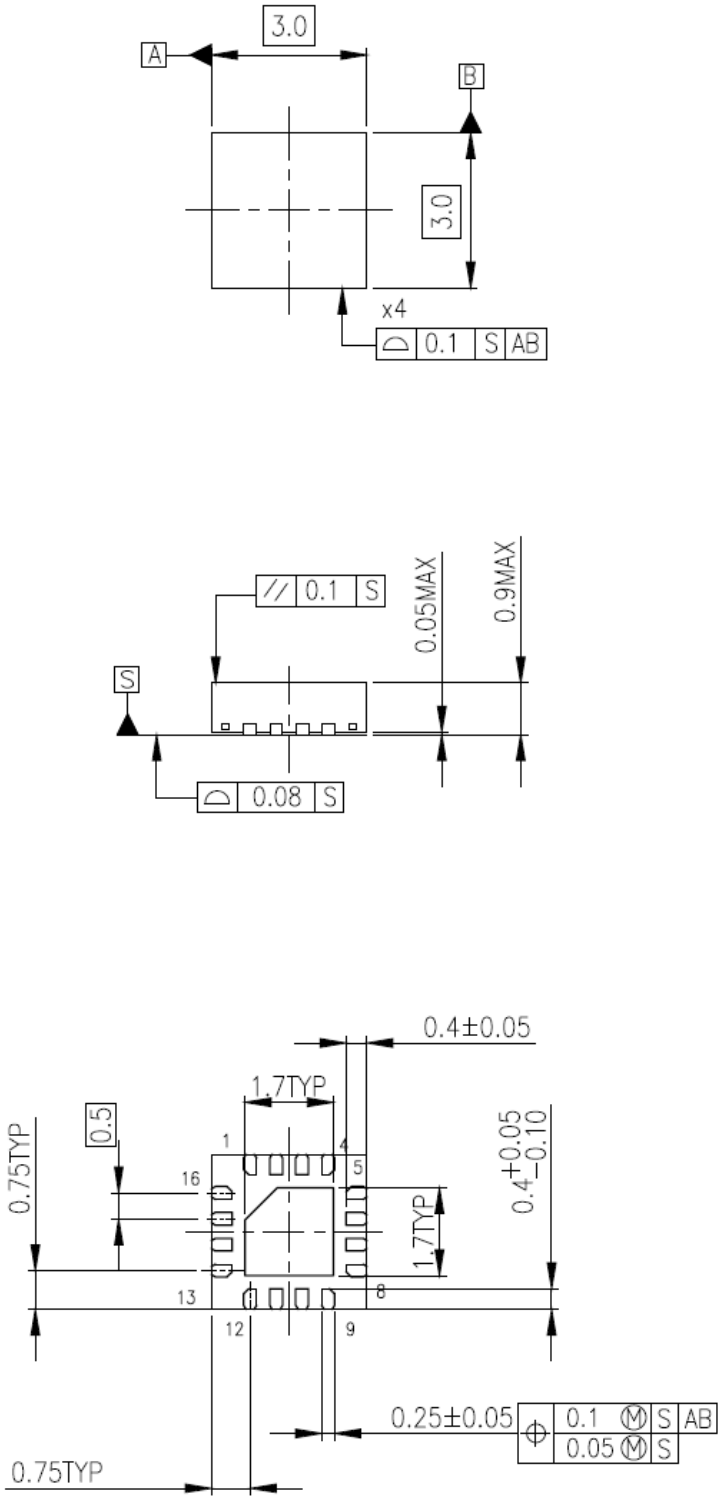


Figure 18.1 Package Dimensions (P-VQFN16-0303-0.50-001)

Weight: 0.02 g (typ.)

18.2. Package Dimensions (P-HTSSOP16-0505-0.65-002)

Unit: mm

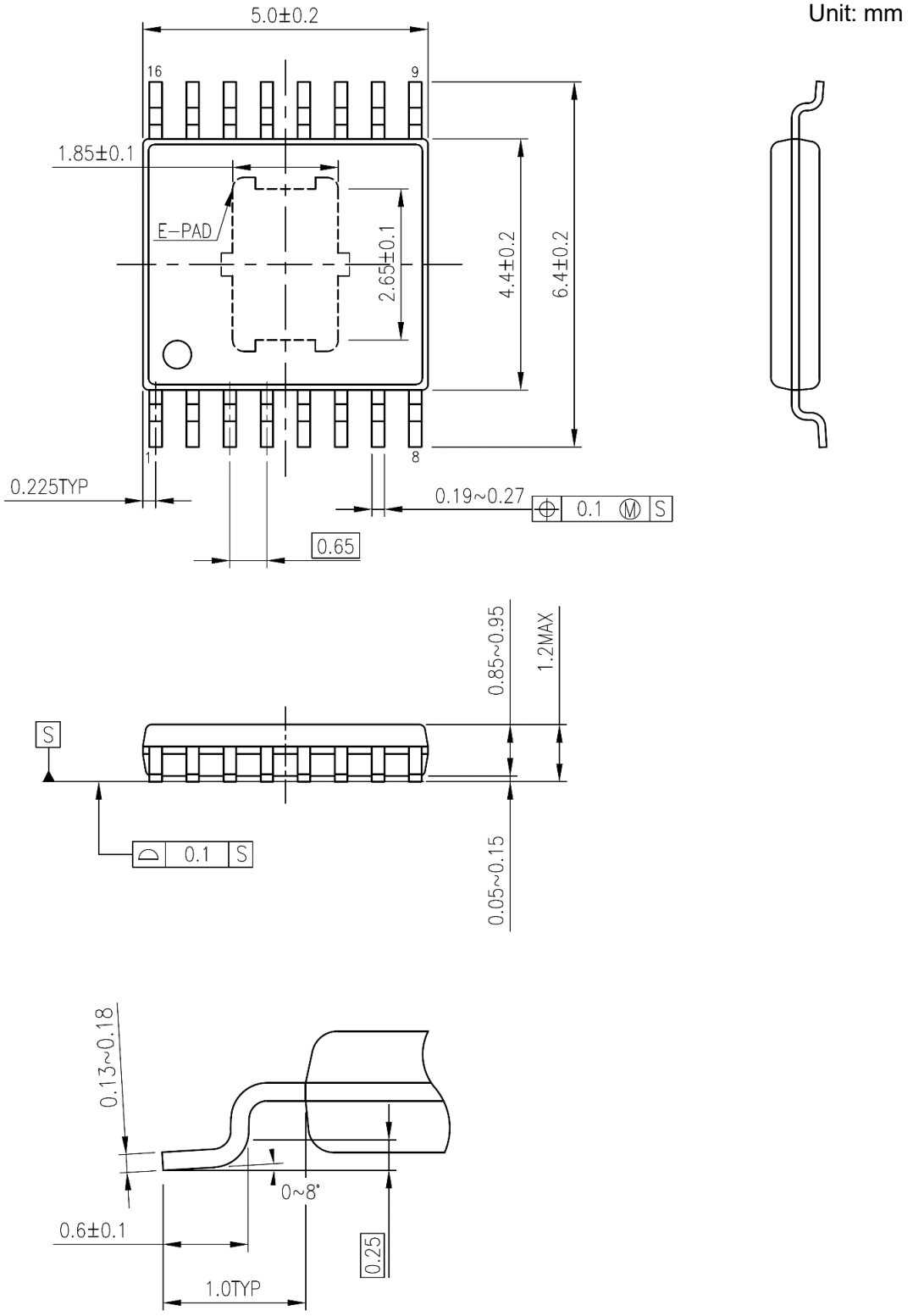


Figure 18.2 Package Dimensions (P-HTSSOP16-0505-0.65-002)

Weight: 0.06 g (typ.)

19. Note on Contents

19.1. Block Diagrams

Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes.

19.2. Equivalent Circuits

The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

19.3. Timing Charts

Timing charts may be simplified for explanatory purposes.

19.4. Application Circuit Example

The application circuits shown in this document are provided for reference purposes only. Thorough evaluation is required, especially at the mass production design stage.
Providing these application circuit examples does not grant a license for industrial property rights.

20. IC Usage Considerations

20.1. Notes on Handling of ICs

(1) The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings.
Exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.

(2) Do not insert devices in the wrong orientation or incorrectly.
Make sure that the positive and negative terminals of power supplies are connected properly.
Otherwise, the current or power consumption may exceed the absolute maximum rating, and exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.
In addition, do not use any device that is applied the current with inserting in the wrong orientation or incorrectly even just one time.

(3) Use an appropriate power supply fuse to ensure that a large current does not continuously flow in case of over-current and/or IC failure. The IC will fully break down when used under conditions that exceed its absolute maximum ratings, when the wiring is routed improperly or when an abnormal pulse noise occurs from the wiring or load, causing a large current to continuously flow and the breakdown can lead smoke or ignition. To minimize the effects of the flow of a large current in case of breakdown, appropriate settings, such as fuse capacity, fusing time and insertion circuit location, are required.

(4) If your design includes an inductive load such as a motor coil, incorporate a protection circuit into the design to prevent device malfunction or breakdown caused by the current resulting from the inrush current at power ON or the negative current resulting from the back electromotive force at power OFF. IC breakdown may cause injury, smoke or ignition.
Use a stable power supply with ICs with built-in protection functions. If the power supply is unstable, the protection function may not operate, causing IC breakdown. IC breakdown may cause injury, smoke or ignition.

(5) Carefully select external components (such as inputs and negative feedback capacitors) and load components (such as speakers), for example, power amp and regulator.
If there is a large amount of leakage current such as input or negative feedback condenser, the IC output DC voltage will increase. If this output voltage is connected to a speaker with low input withstand voltage, over-current or IC failure can cause smoke or ignition. (The over-current can cause smoke or ignition from the IC itself.) In particular, please pay attention when using a Bridge Tied Load (BTL) connection type IC that inputs output DC voltage to a speaker directly.

21. Points to Remember on Handling of ICs

(1) Over-current detection circuit

Over-current detection circuits (referred to as current limiter circuits) do not necessarily protect ICs under all circumstances. If the over-current protection circuits operate against the over-current, clear the over-current status immediately.
Depending on the method of use and usage conditions, such as exceeding absolute maximum ratings can cause the over-current protection circuit to not operate properly or IC breakdown before operation. In addition, depending on the method of use and usage conditions, if over-current continues to flow for a long time after operation, the IC may generate heat resulting in breakdown.

(2) Thermal shutdown circuit

Thermal shutdown circuits do not necessarily protect ICs under all circumstances. If the thermal shutdown circuits operate against the over temperature, clear the heat generation status immediately.
Depending on the method of use and usage conditions, such as exceeding absolute maximum ratings can cause the thermal shutdown circuit to not operate properly or IC breakdown before operation.

(3) Heat radiation design

In using an IC with large current flow such as power amp, regulator or driver, please design the device so that heat is appropriately radiated, not to exceed the specified junction temperature (Tj) at any time and condition. These ICs generate heat even during normal use. An inadequate IC heat radiation design can lead to decrease in IC life, deterioration of IC characteristics or IC breakdown. In addition, please design the device taking into considerate the effect of IC heat radiation with peripheral components.

(4) Back-EMF

When a motor reverses the rotation direction, stops or slows down abruptly, a current flow back to the motor’s power supply due to the effect of back-EMF. If the current sink capability of the power supply is small, the device’s motor power supply and output pins might be exposed to conditions beyond absolute maximum ratings. To avoid this problem, take the effect of back-EMF into consideration in system design.

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